**CS 223 Fall 2015 Lab Projects (v. 2)**

1 - The project will be done by teams of 2 students. You may choose to work with the person who is your lab partner, or choose a different partner for the project. If a project partner leaves the course for some reason (serious illness, W grade, gives up, etc.) the other student must continue without him/her and complete the project by themself.

2 - The contents of the project will be decided by each group. However there are few restrictions:

(i) The project should use the BASYS2 board and at least one of the modules on the Beti experiment board.

(ii) The project should have a Verilog HDL component, implemented on the FPGA.

(iii) The project must contain a control section and a data processing section (based on the controller + datapath model of our course).

(iv) Projects should not be copies of existing projects. (i.e some books have chapters on how to connect a mouse or a keyboard to a FPGA. The book also has code written in Verilog). Pre-written codes may be used in the project if you are adding a significant amount of extra work. If such code (from a book, Internet, or whereever) is used, it should be referenced in your project reports.

3 - Ideas for projects can come from your or your partner’s imagination, family and friends, news items, YouTube, the Internet, books, magazines, etc. Things that interest you (such as games, or information processing, or music) can be topics. Inputs can be sensors (microphones, fingerprint readers, motion detectors, etc), keyboard, keypad, mouse, buttons/switches, even pre-stored data from memory. Outputs can be motors, display devices, speakers, actuators, etc. Let your imagination soar!

4 - Your project may involve more than the BASYS2 board and the CS223 Beti experiment board. You may use additional chips (A/D, D/A, memory, interface, drivers, etc), additional boards (more than one BASYS2, other FPGA boards (e.g. BASYS3), the CS224 Beti board and its I/O devices, more than one CS223 Beti board, etc) and any peripheral devices for input and output that you want. Lots of interesting things are available in the electronics stores of Kizilay and Ulus !

5 - Each group should prepare a short Project Proposal, at most two A4 pages, following the specifications given below. To receive full credit, it must be uploaded to the Unilica Assignment before *November 2, 2015*. Although late proposals will be accepted they will lose some points after *November 9, 2015* . No proposal will be accepted after *November 16, 2015.*

6 - Each group will submit a short Progress Report to Unilica Assignment, due *December 1 2015*. The report should include project proposal and an outline of the progress so far. It should also outline the work to be done in the future. The report should be at most three pages long excluding the project proposal.

7 - The projects should be completed by *December 21,2015* and a short Final Project Report describing the project and its implementation should be uploaded to the Unilica Assignment. The report will contain the self-documenting Verilog code (with explanatory headers, line comments, etc). The report should include references to all the external material and sources used in the project.

8 - Students will demonstrate their projects to the instructor and the TA’s in the week of *December 21, 2015*. At this demo, there will be a code review and oral exam, to determine how much of the project each partner has done and/or understands, and how much of the project is working as proposed, and how much the project adheres to the original proposal (or exceeds it).

9 - Grading will be as follows:

(i) Project proposal: 25% Clarity and quality of the proposal document, and originality of the idea are the determinants of the grade.

(ii) Progress report: 25% Clarity and quality of the progress report document, the answers to the oral interview, and the amount of progress made will determine the grade.

(iii) Final report: 40% Clarity and quality of the final report document, quality of the demo and overall design, and completeness of the implementation will determine the grade.

(iv) Peer grading: 10% Group members will give peer grades to each other.

Project Proposal

The Project Proposal is a short report, at most 2 pages. It should contain the following information, in 4 distinct sections of the report:

1. Project name, Section #, (if the same as in lab) Group #, names and ID #s of the students in the project group
2. Description of the project: tell what is it, what will it do, what the behavior of it will be, etc. Be clear in specifying the inputs, the outputs and their funtional relationship.
3. Equipment to be used: in a list form, state which FPGA board(s) and which hardware on the FPGA board(s), which Beti lab boards and which I/O modules on the Beti boards, which additional chips, which additional external I/O devices, etc. will be used. [Note: if components are needed which are not available in the lab, students should buy them from electronics stores.]
4. Deliverables: a “deliverable” is something you will you submit or show during the course of the project. List all the deliverables and their due dates, of everything you will give during this project, up to and including the demo day. These will include all the reports, the Verilog code, a short oral presentation about your project, the demo of your project in use, etc.